ABSTRACT

A method and apparatus for providing a plurality of aligned instructions from an instruction stream provided by a memory unit for execution within a pipelined microprocessor is described. The microprocessor comprises a prefetch buffer, whereby the prefetch buffer stores prefetched instructions and additional information about the validity and size of the prefetch buffer. The method and apparatus use the prefetch buffer to buffer a part of an instruction stream. The actually aligned instruction stream is issued from the prefetch buffer or directly by instructions fetched from the memory, or from a combination of prefetched instructions and actually fetched instructions.